Fig.1

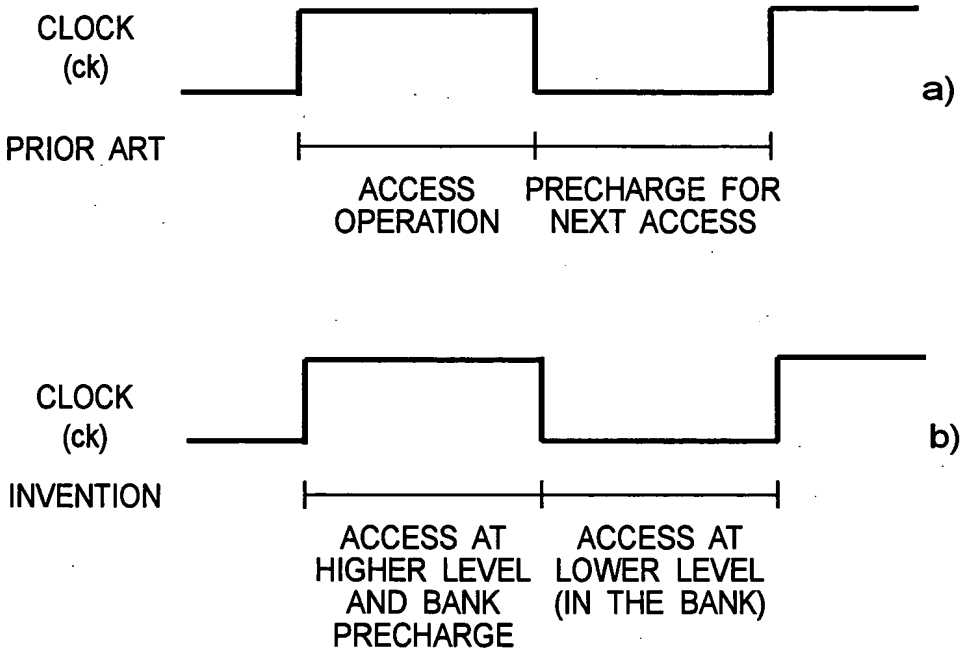

CLOCK
(ck)
a)
PRIOR ART
ACCESS OPERATION
PRECHARGE FOR NEXT ACCESS
CLOCK
(ck)
b)
INVENTION
ACCESS AT HIGHER LEVEL AND BANK PRECHARGE
ACCESS AT LOWER LEVEL (IN THE BANK)

Fig.2

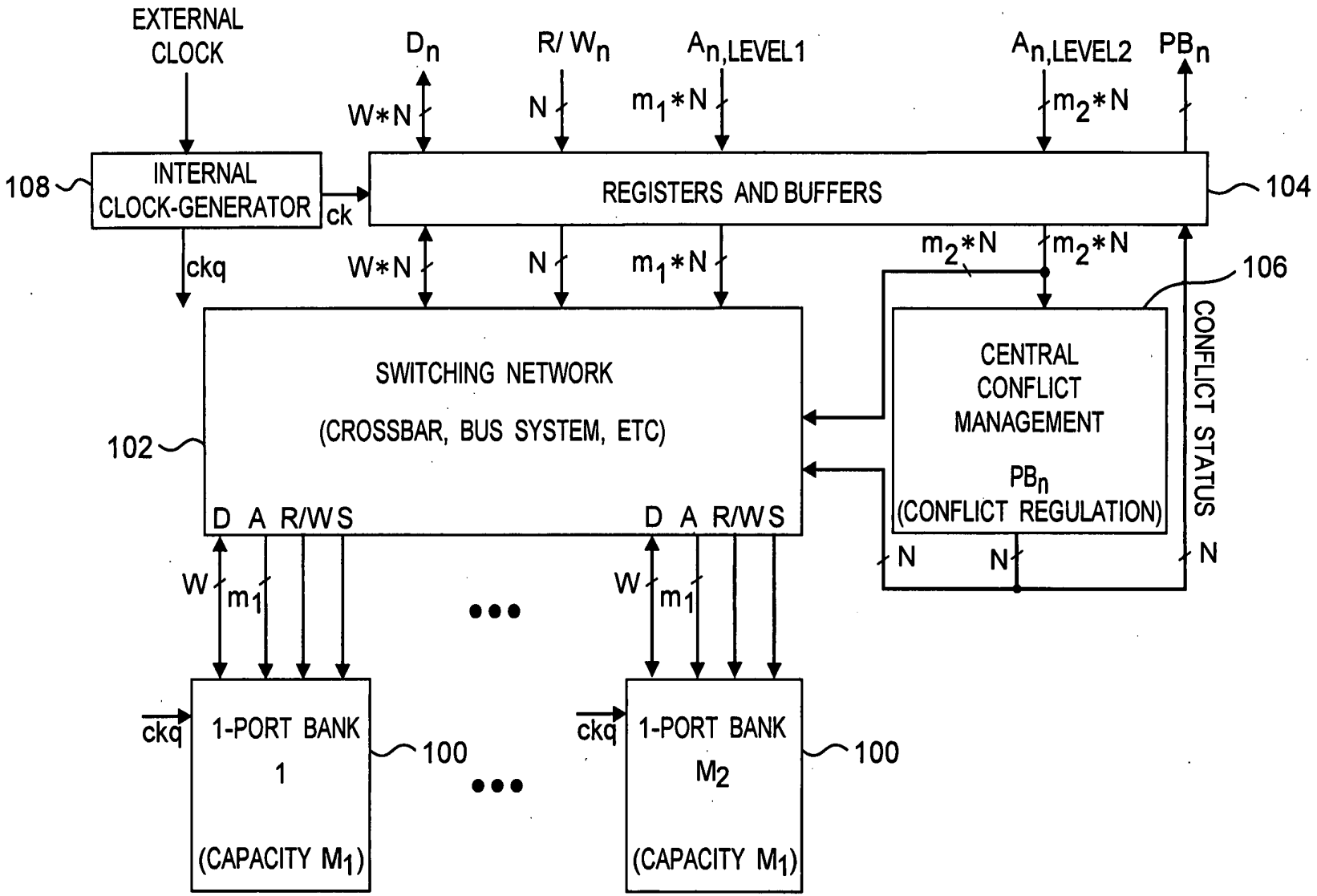

EXTERNAL CLOCK
D_n
R/ W_n
$A_{n,LEVEL1}$
$A_{n,LEVEL2}$
PB_n
W*N
N
m_1*N
m_2*N
108
INTERNAL CLOCK-GENERATOR
ck
REGISTERS AND BUFFERS
104
ckq
W*N
N
m_1*N
m_2*N
m_2*N
106
CONFLICT STATUS
SWITCHING NETWORK
(CROSSBAR, BUS SYSTEM, ETC)
102
CENTRAL CONFLICT MANAGEMENT
PB_n
(CONFLICT REGULATION)
D A R/W S
D A R/W S
N
N
N
W
m_1
W
m_1
ckq
1-PORT BANK 1
(CAPACITY M_1)
100
ckq
1-PORT BANK M_2
(CAPACITY M_1)
100

Fig.3

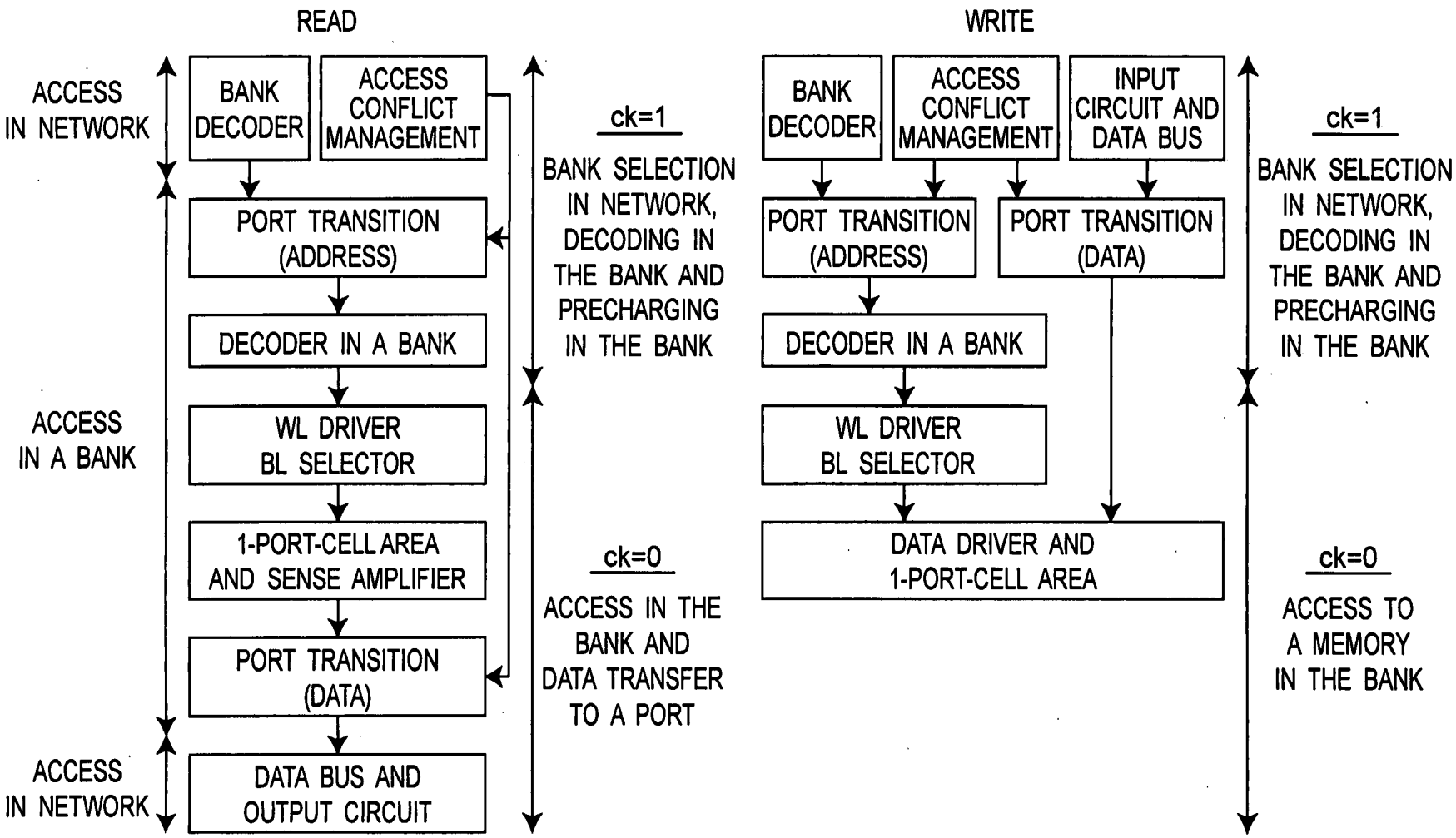

READ
WRITE
ACCESS IN NETWORK
ACCESS IN A BANK
ACCESS IN NETWORK
BANK DECODER
ACCESS CONFLICT MANAGEMENT
INPUT CIRCUIT AND DATA BUS
PORT TRANSITION (ADDRESS)
PORT TRANSITION (DATA)
DECODER IN A BANK
WL DRIVER BL SELECTOR
1-PORT-CELL AREA AND SENSE AMPLIFIER
DATA DRIVER AND 1-PORT-CELL AREA
DATA BUS AND OUTPUT CIRCUIT
ck=1
BANK SELECTION IN NETWORK, DECODING IN THE BANK AND PRECHARGING IN THE BANK
ck=0
ACCESS IN THE BANK AND DATA TRANSFER TO A PORT
ACCESS TO A MEMORY IN THE BANK

Fig.4

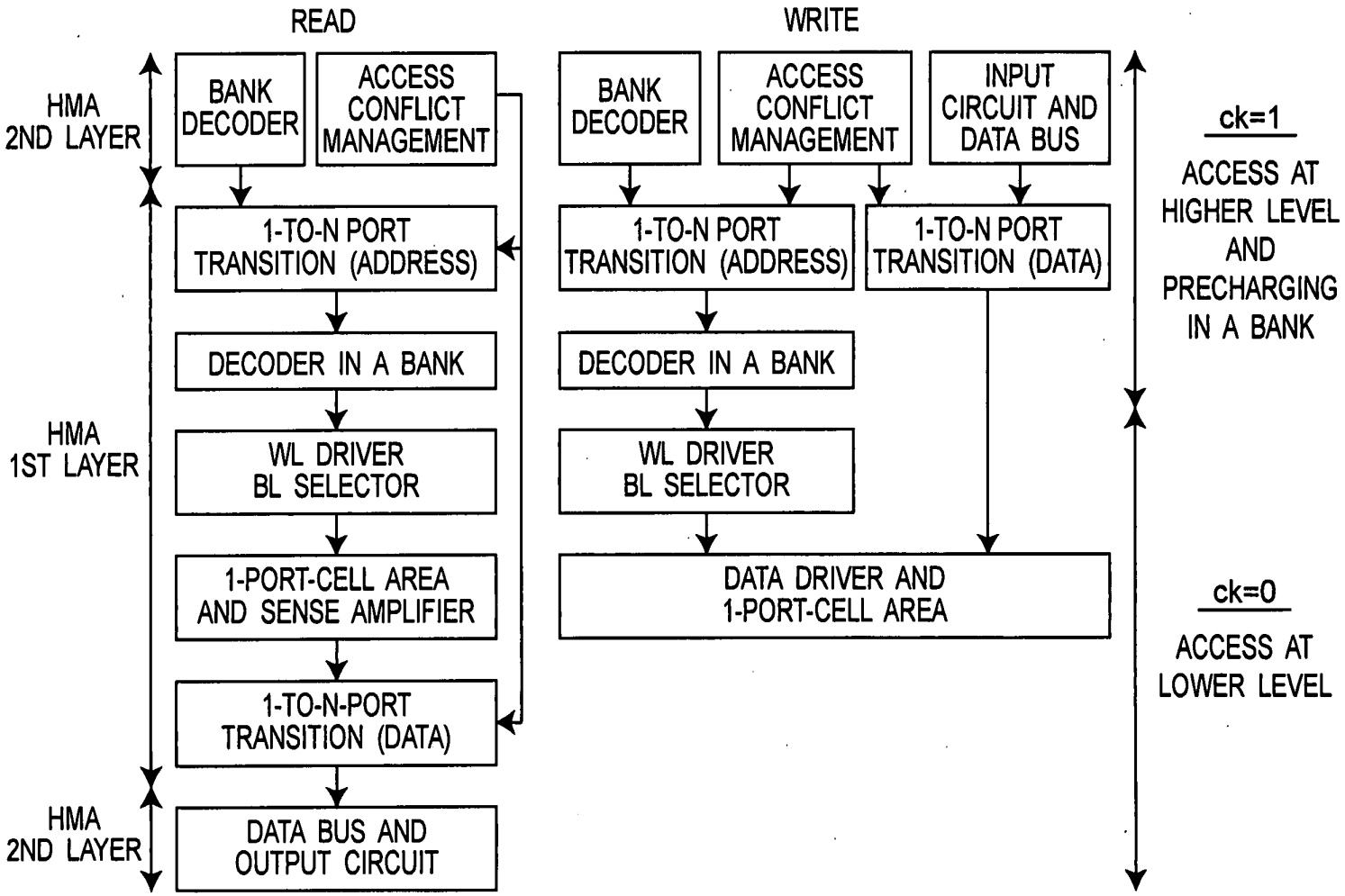

READ
WRITE
HMA 2ND LAYER
HMA 1ST LAYER
HMA 2ND LAYER
BANK DECODER
ACCESS CONFLICT MANAGEMENT
INPUT CIRCUIT AND DATA BUS
1-TO-N PORT TRANSITION (ADDRESS)
1-TO-N PORT TRANSITION (DATA)
DECODER IN A BANK
WL DRIVER BL SELECTOR
1-PORT-CELL AREA AND SENSE AMPLIFIER
DATA DRIVER AND 1-PORT-CELL AREA
1-TO-N-PORT TRANSITION (DATA)
DATA BUS AND OUTPUT CIRCUIT
ck=1
ACCESS AT HIGHER LEVEL AND PRECHARGING IN A BANK
ck=0
ACCESS AT LOWER LEVEL

Fig.5

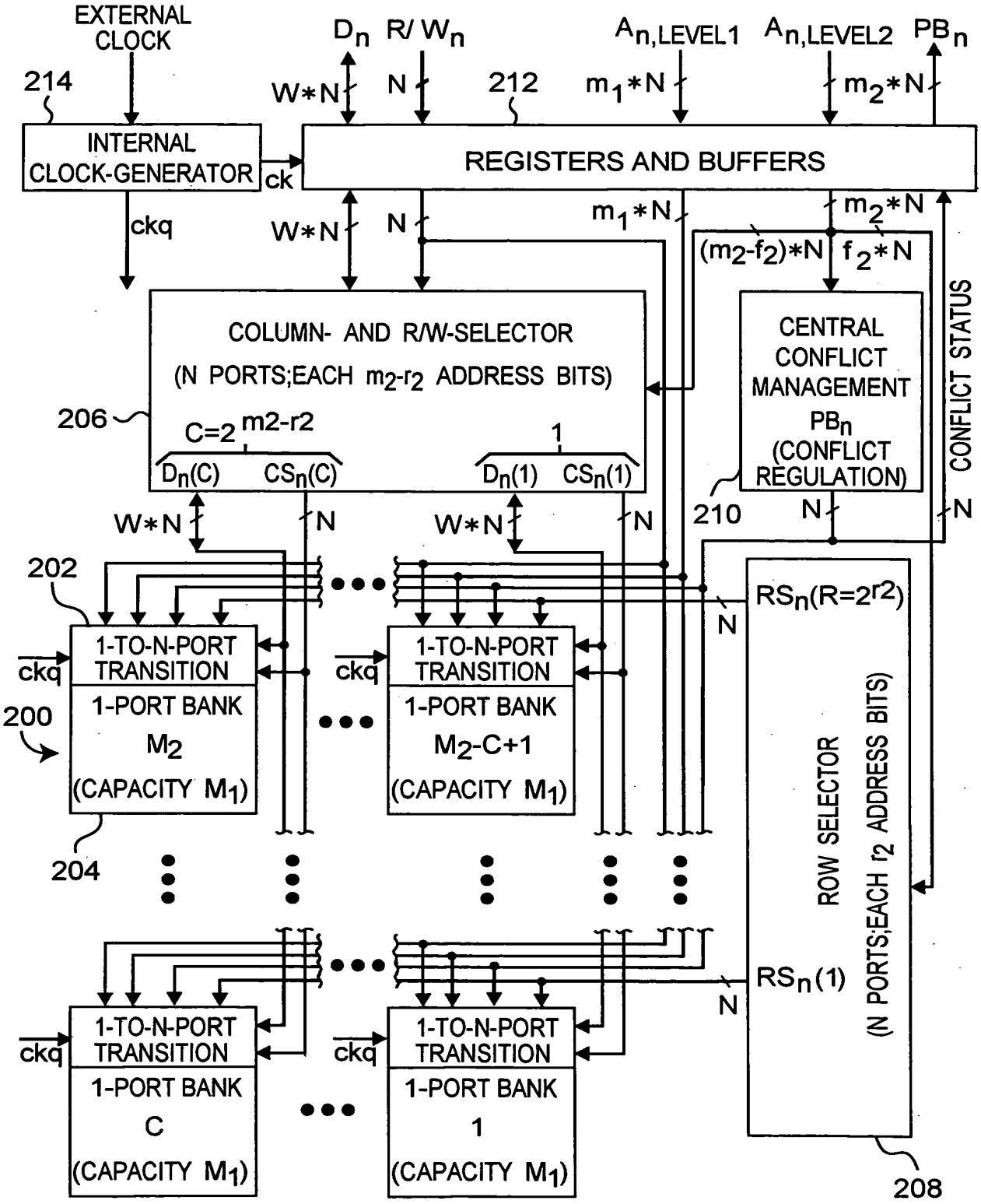

EXTERNAL CLOCK
214
INTERNAL CLOCK-GENERATOR
ck
ckq
D_n R/ W_n
W*N
N
212
REGISTERS AND BUFFERS
$A_{n,LEVEL1}$
m_1*N
$A_{n,LEVEL2}$
m_2*N
PB_n
m_1*N
m_2*N
(m_2-f_2)*N
f_2*N
CONFLICT STATUS
COLUMN- AND R/W-SELECTOR
(N PORTS;EACH m_2-r_2 ADDRESS BITS)
206
C=2 m2-r2
1
$D_n(C)$ $CS_n(C)$
$D_n(1)$ $CS_n(1)$
CENTRAL CONFLICT MANAGEMENT
PB_n
(CONFLICT REGULATION)
210
202
1-TO-N-PORT TRANSITION
1-PORT BANK
M_2
(CAPACITY M_1)
200
204
M_2-C+1
C
1
$RS_n(R=2^{r2})$
$RS_n(1)$
ROW SELECTOR
(N PORTS;EACH r_2 ADDRESS BITS)
208

Fig.6

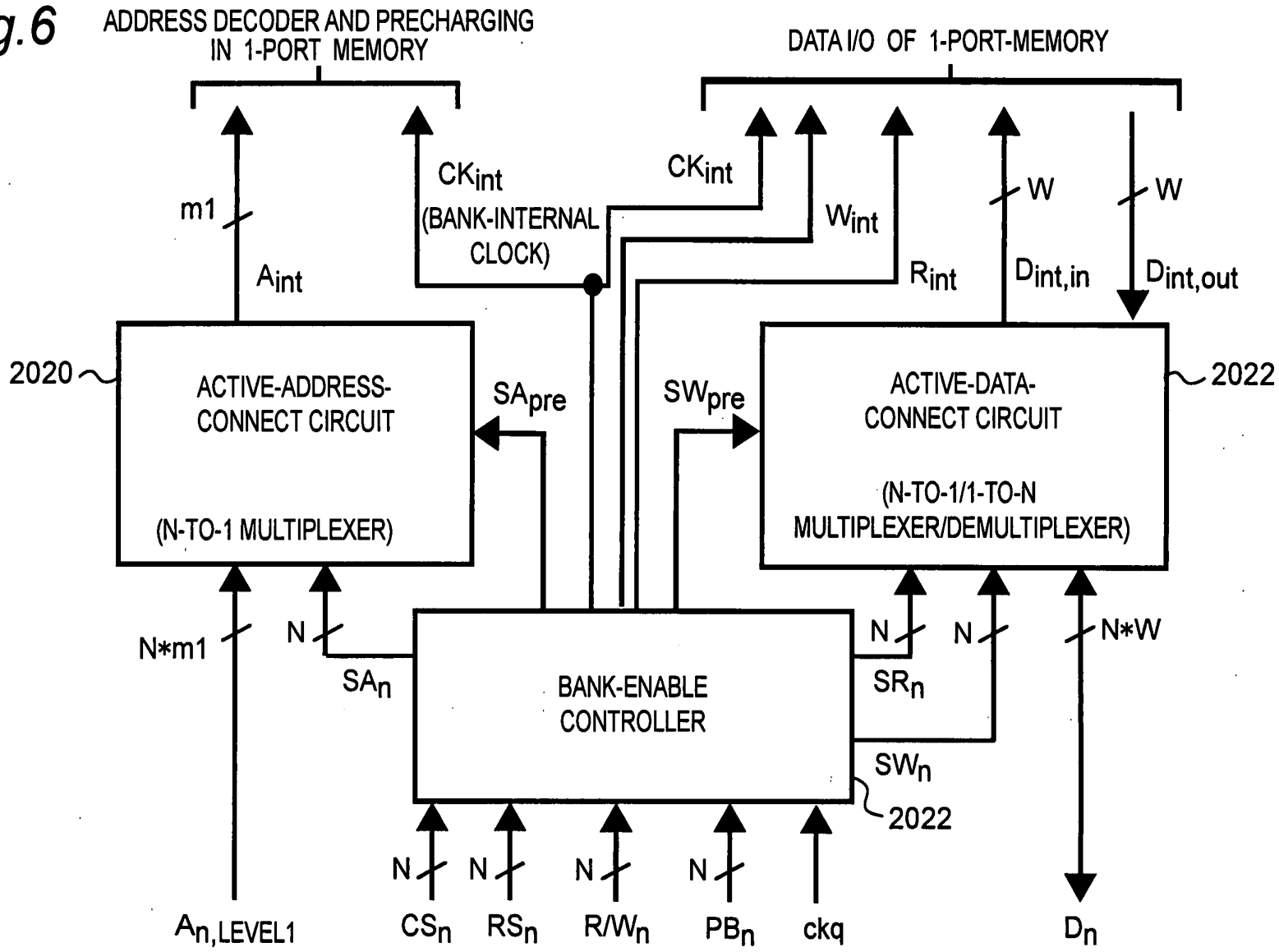

ADDRESS DECODER AND PRECHARGING IN 1-PORT MEMORY
DATA I/O OF 1-PORT-MEMORY
m1
Aint
CKint (BANK-INTERNAL CLOCK)
CKint
Wint
Rint
W
Dint,in
W
Dint,out
2020
ACTIVE-ADDRESS-CONNECT CIRCUIT
(N-TO-1 MULTIPLEXER)
SApre
SWpre
ACTIVE-DATA-CONNECT CIRCUIT
(N-TO-1/1-TO-N MULTIPLEXER/DEMULTIPLEXER)
2022
N*m1
N
SAn
BANK-ENABLE CONTROLLER
N
SRn
N
N*W
SWn
2022
N
N
N
N
An,LEVEL1
CSn
RSn
R/Wn
PBn
ckq
Dn

Fig.7

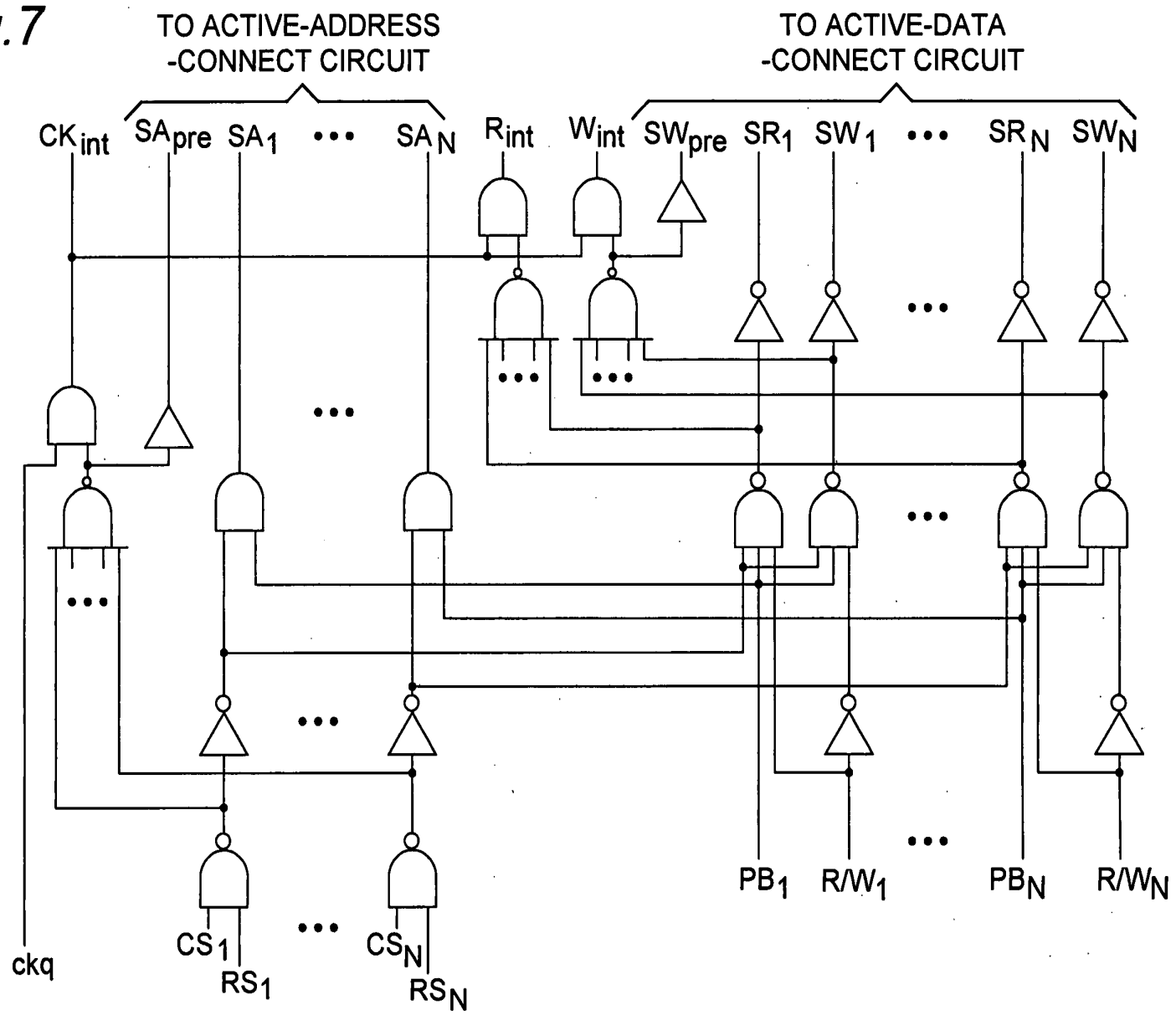

TO ACTIVE-ADDRESS
-CONNECT CIRCUIT
TO ACTIVE-DATA
-CONNECT CIRCUIT
CK int
SA pre
SA 1
SA N
R int
W int
SW pre
SR 1
SW 1
SR N
SW N
PB 1
R/W 1
PB N
R/W N
ckq
CS 1
RS 1
CS N
RS N

Fig.8

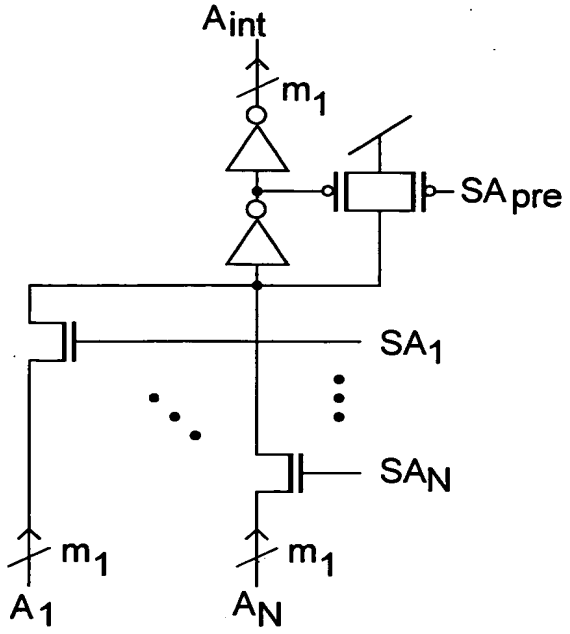

Aint
m1
SApre
SA1
SAN
m1
m1
A1
AN

Fig.9

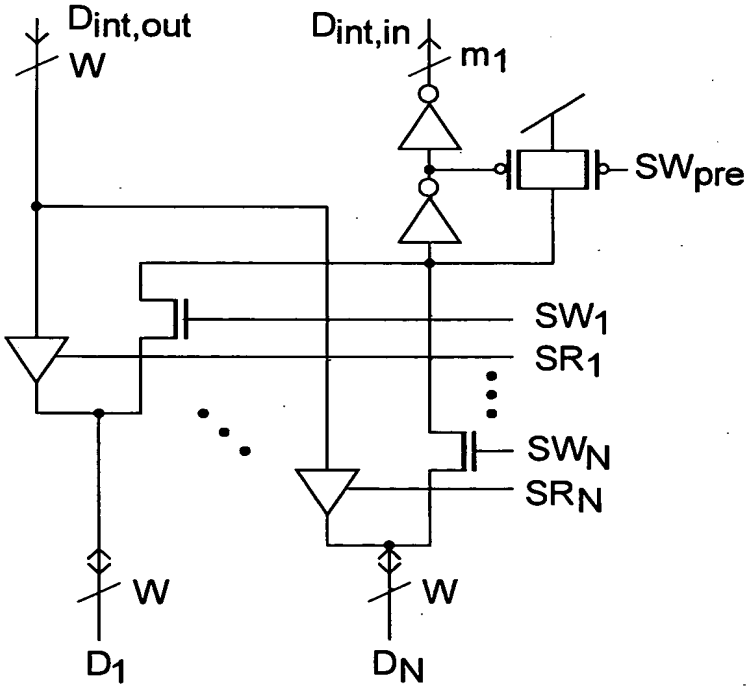

Dint,out
W
Dint,in
m1
SWpre
SW1
SR1
SWN
SRN
W
W
D1
DN

Fig.10

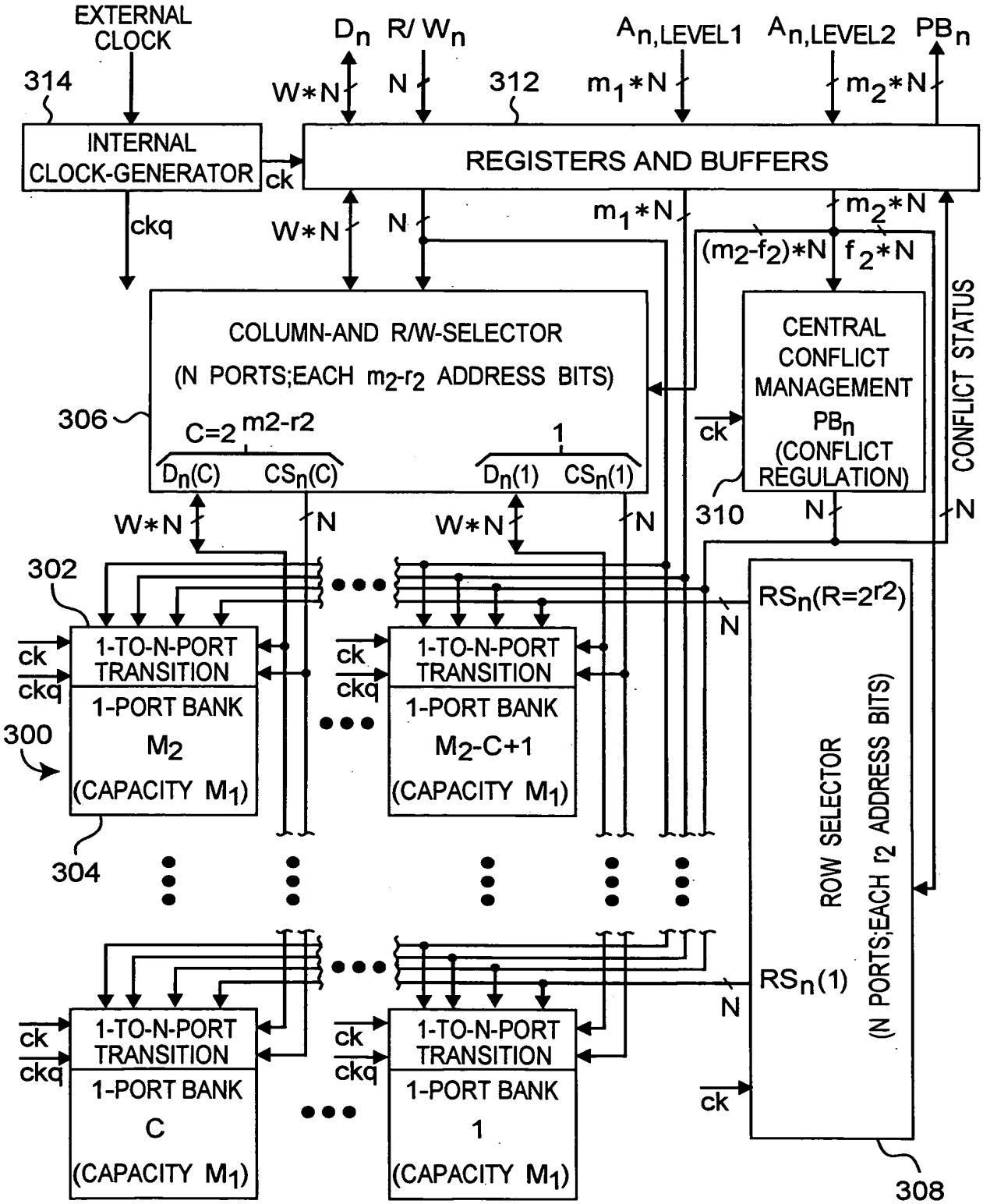

EXTERNAL CLOCK
314
INTERNAL CLOCK-GENERATOR
ck
ckq
D_n R/ W_n
W*N
N
312
$A_{n,LEVEL1}$
$A_{n,LEVEL2}$
PB_n
m_1*N
m_2*N
REGISTERS AND BUFFERS
(m_2-f_2)*N
f_2*N
CONFLICT STATUS
COLUMN-AND R/W-SELECTOR
(N PORTS;EACH m_2-r_2 ADDRESS BITS)
306
C=2 m2-r2
1
$D_n(C)$ $CS_n(C)$
$D_n(1)$ $CS_n(1)$
CENTRAL CONFLICT MANAGEMENT PB_n (CONFLICT REGULATION)
310
302
1-TO-N-PORT TRANSITION
1-PORT BANK
M_2
(CAPACITY M_1)
300
304
M_2-C+1
C
1
$RS_n(R=2^{r2})$
$RS_n(1)$
ROW SELECTOR
(N PORTS;EACH r_2 ADDRESS BITS)
308

Fig.11

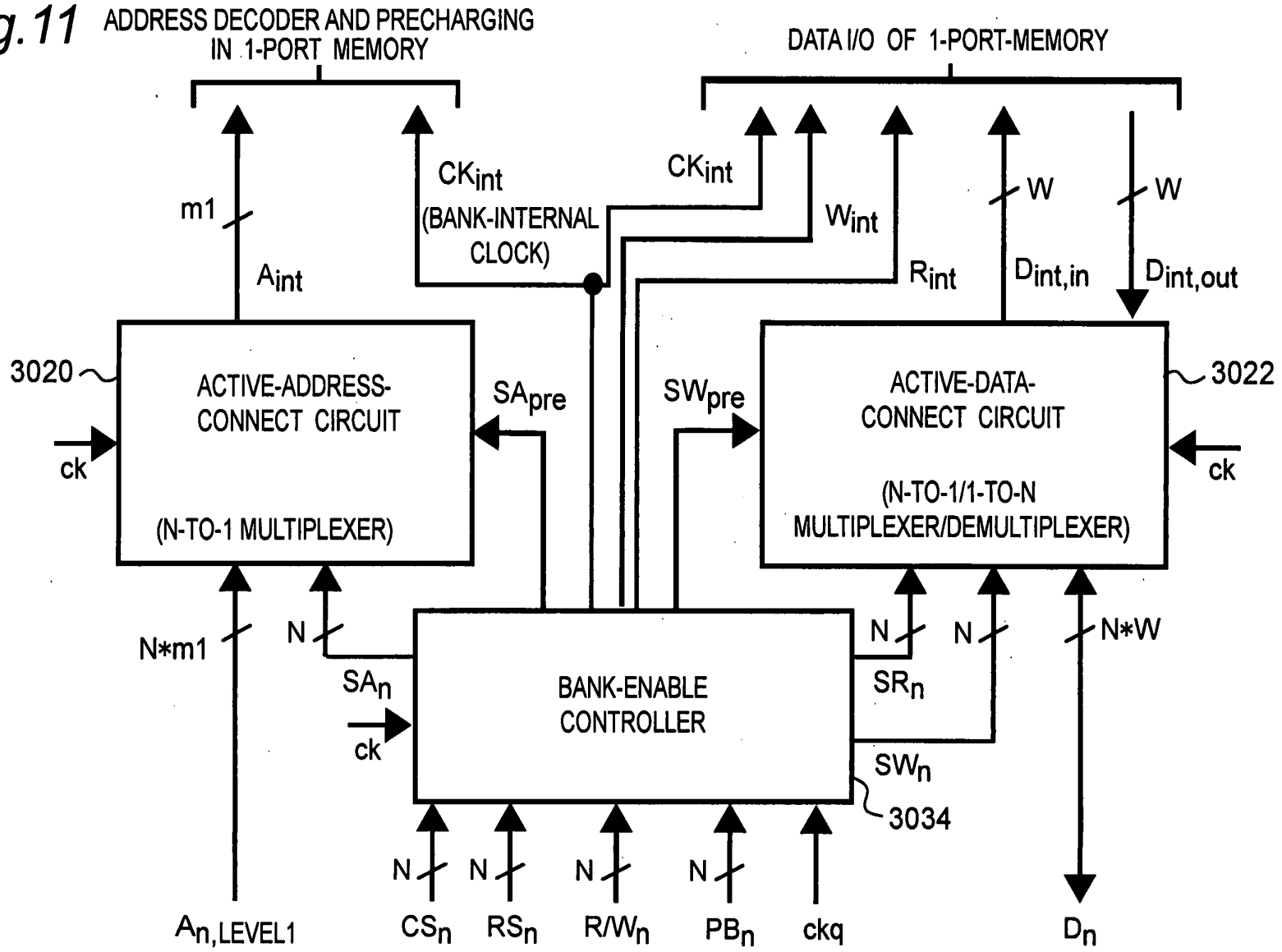

ADDRESS DECODER AND PRECHARGING IN 1-PORT MEMORY
DATA I/O OF 1-PORT-MEMORY
m1
Aint
CKint (BANK-INTERNAL CLOCK)
CKint
Wint
Rint
W
Dint,in
W
Dint,out
3020
ACTIVE-ADDRESS-CONNECT CIRCUIT
(N-TO-1 MULTIPLEXER)
ck
SApre
SWpre
ACTIVE-DATA-CONNECT CIRCUIT
(N-TO-1/1-TO-N MULTIPLEXER/DEMULTIPLEXER)
3022
ck
N*m1
N
SAn
ck
BANK-ENABLE CONTROLLER
N
SRn
N
SWn
3034
N*W
N
CSn
N
RSn
N
R/Wn
N
PBn
ckq
An,LEVEL1
Dn

Fig.12

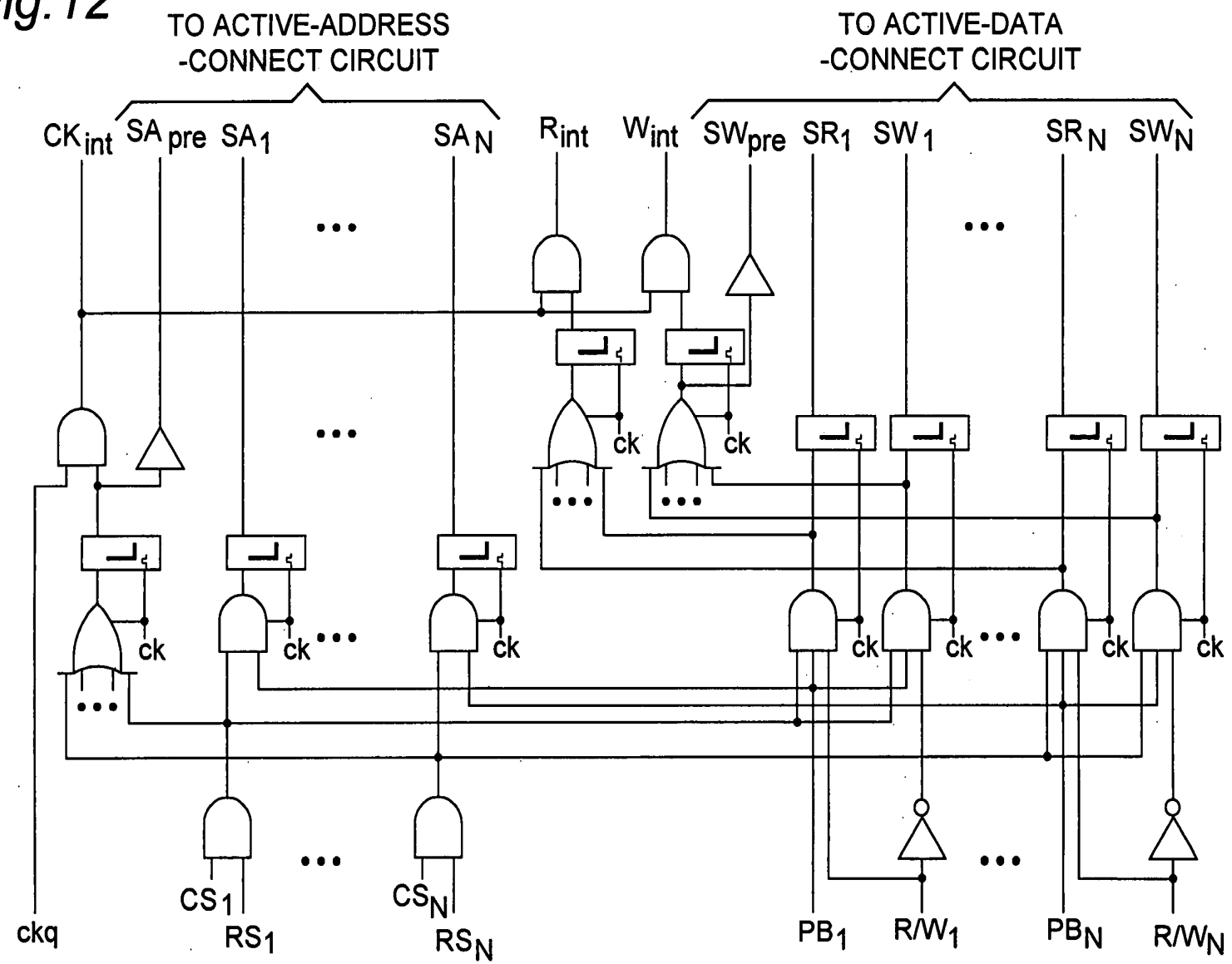

TO ACTIVE-ADDRESS
-CONNECT CIRCUIT
TO ACTIVE-DATA
-CONNECT CIRCUIT
CK int
SA pre
SA 1
SA N
R int
W int
SW pre
SR 1
SW 1
SR N
SW N
ck
ckq
CS 1
RS 1
CS N
RS N
PB 1
R/W 1
PB N
R/W N

Fig.13

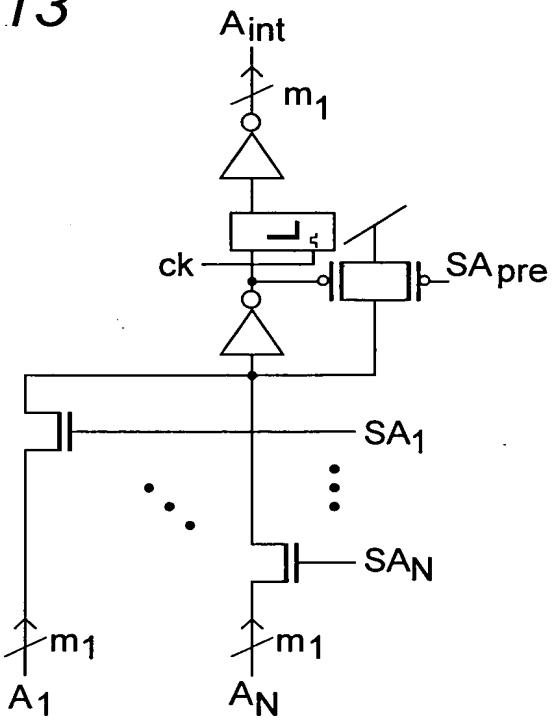

Aint
m1
ck
SApre
SA1
SAN
m1
A1
m1
AN

Fig.14

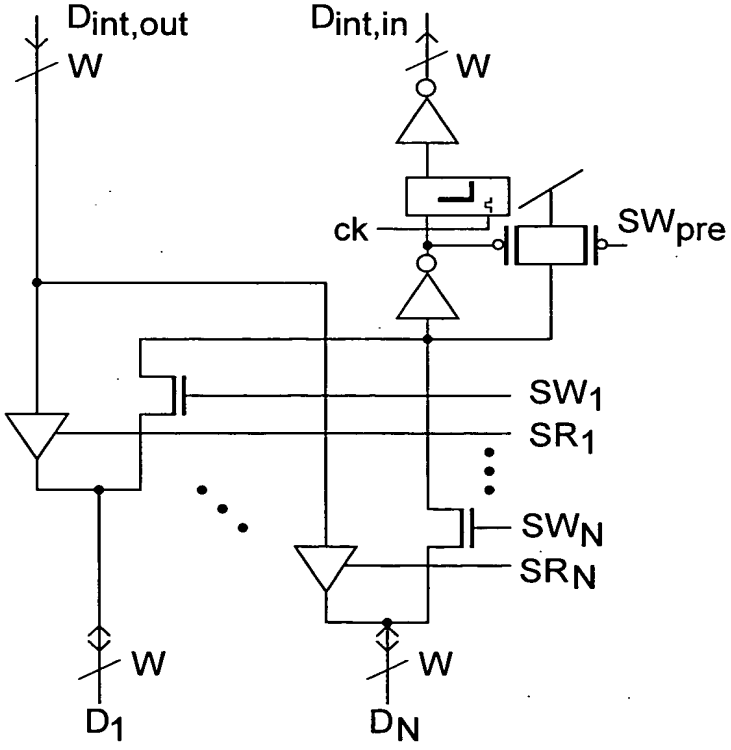

Dint,out
W
Dint,in
W
ck
SWpre
SW1
SR1
SWN
SRN
W
D1
W
DN

Fig.15

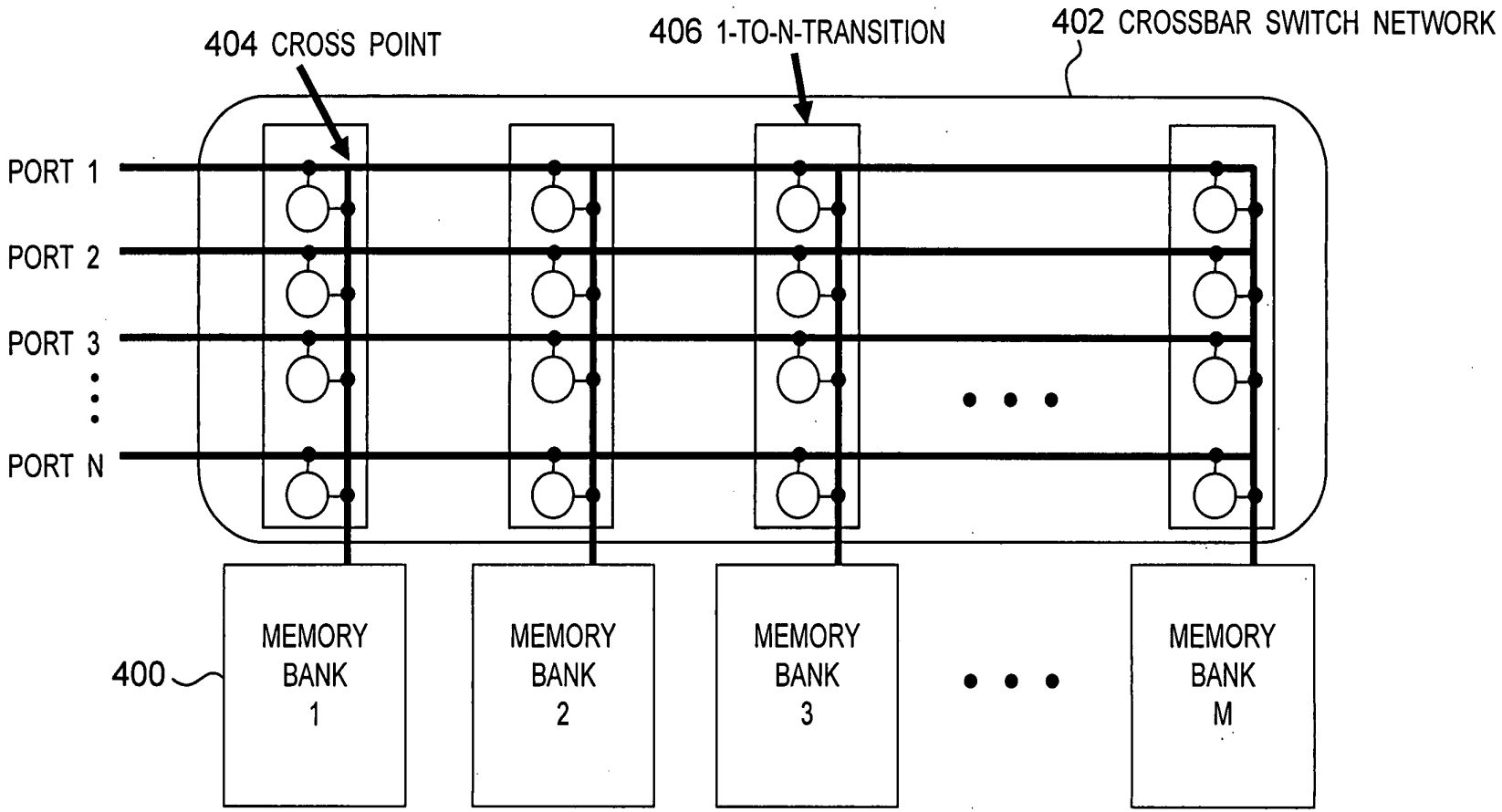

404 CROSS POINT
406 1-TO-N-TRANSITION
402 CROSSBAR SWITCH NETWORK
PORT 1
PORT 2
PORT 3
PORT N
400
MEMORY BANK 1
MEMORY BANK 2
MEMORY BANK 3
MEMORY BANK M

Fig.16

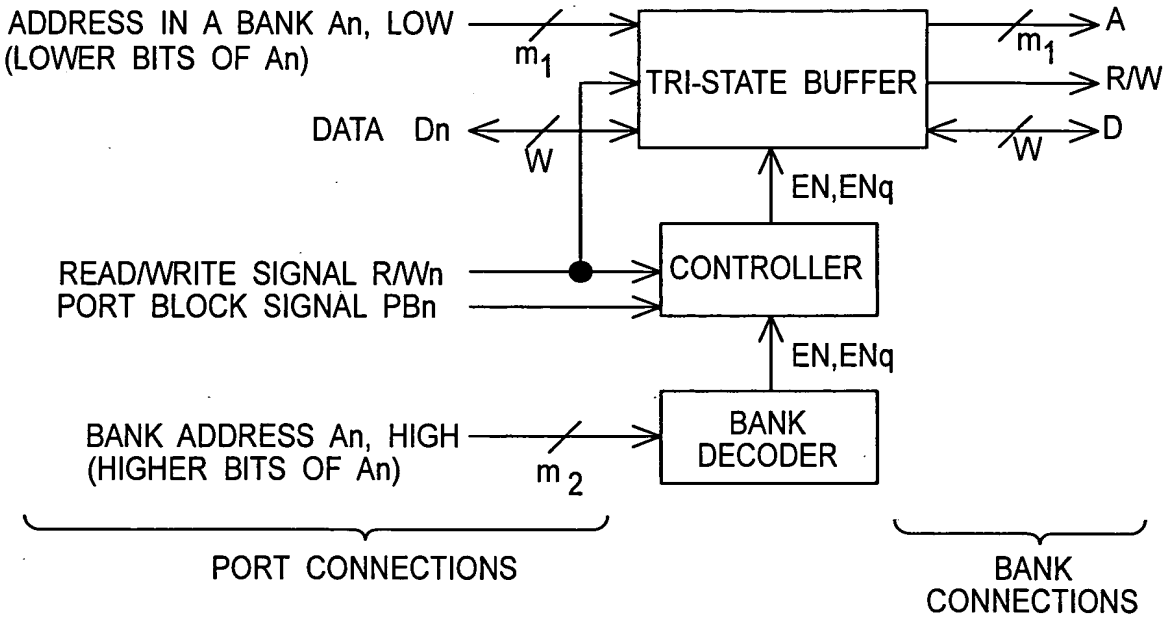

ADDRESS IN A BANK An, LOW
(LOWER BITS OF An)
m1
TRI-STATE BUFFER
m1
A
R/W
DATA Dn
W
W
D
EN,ENq
READ/WRITE SIGNAL R/Wn
PORT BLOCK SIGNAL PBn
CONTROLLER
EN,ENq
BANK ADDRESS An, HIGH
(HIGHER BITS OF An)
m2
BANK
DECODER
PORT CONNECTIONS
BANK
CONNECTIONS

Fig.17

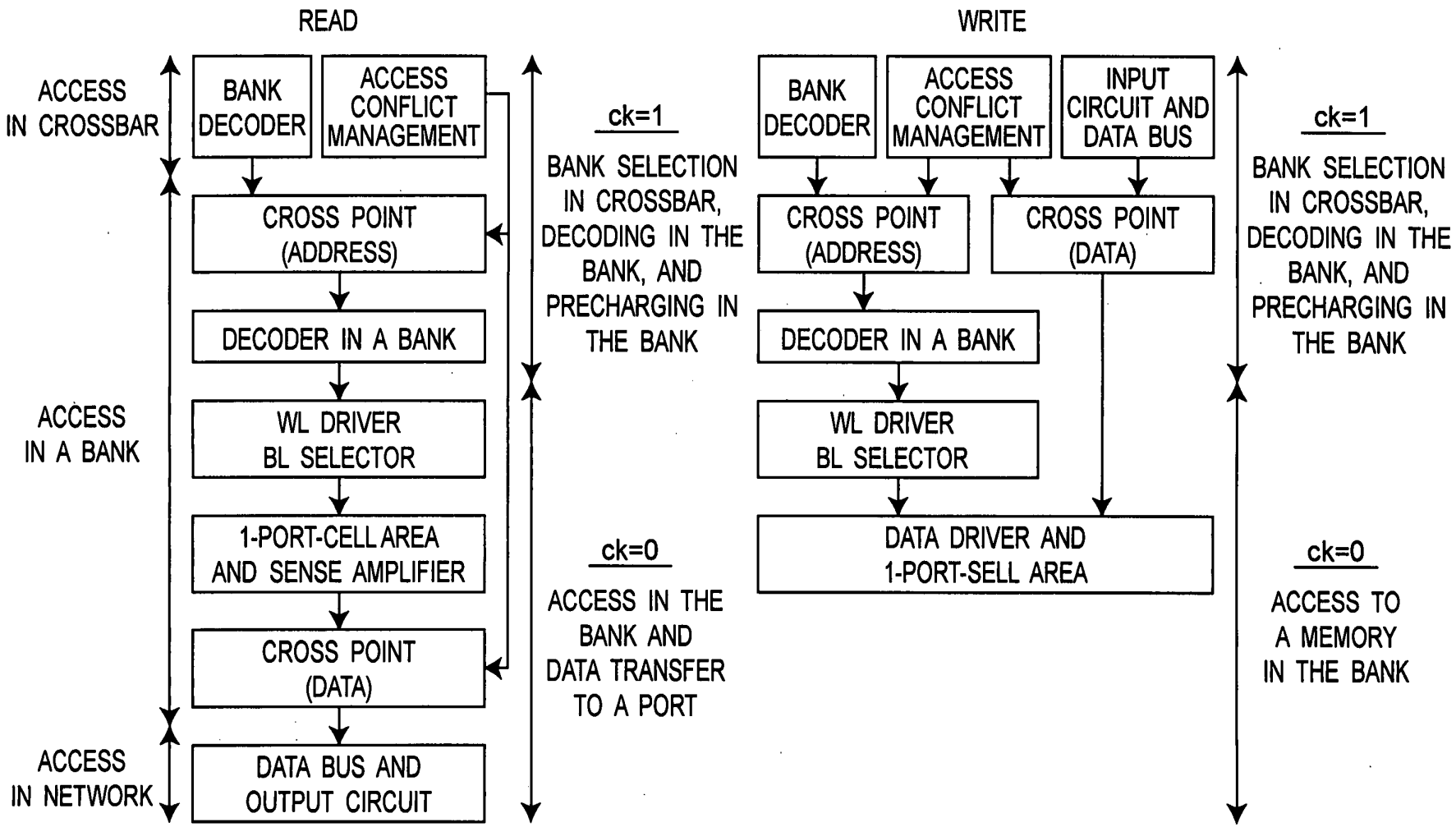

READ
WRITE
ACCESS IN CROSSBAR
ACCESS IN A BANK
ACCESS IN NETWORK
BANK DECODER
ACCESS CONFLICT MANAGEMENT
CROSS POINT (ADDRESS)
DECODER IN A BANK
WL DRIVER BL SELECTOR
1-PORT-CELL AREA AND SENSE AMPLIFIER
CROSS POINT (DATA)
DATA BUS AND OUTPUT CIRCUIT
ck=1
BANK SELECTION IN CROSSBAR, DECODING IN THE BANK, AND PRECHARGING IN THE BANK
ck=0
ACCESS IN THE BANK AND DATA TRANSFER TO A PORT
BANK DECODER
ACCESS CONFLICT MANAGEMENT
INPUT CIRCUIT AND DATA BUS
CROSS POINT (ADDRESS)
CROSS POINT (DATA)
DECODER IN A BANK
WL DRIVER BL SELECTOR
DATA DRIVER AND 1-PORT-SELL AREA
ck=1
BANK SELECTION IN CROSSBAR, DECODING IN THE BANK, AND PRECHARGING IN THE BANK
ck=0
ACCESS TO A MEMORY IN THE BANK

Fig.18

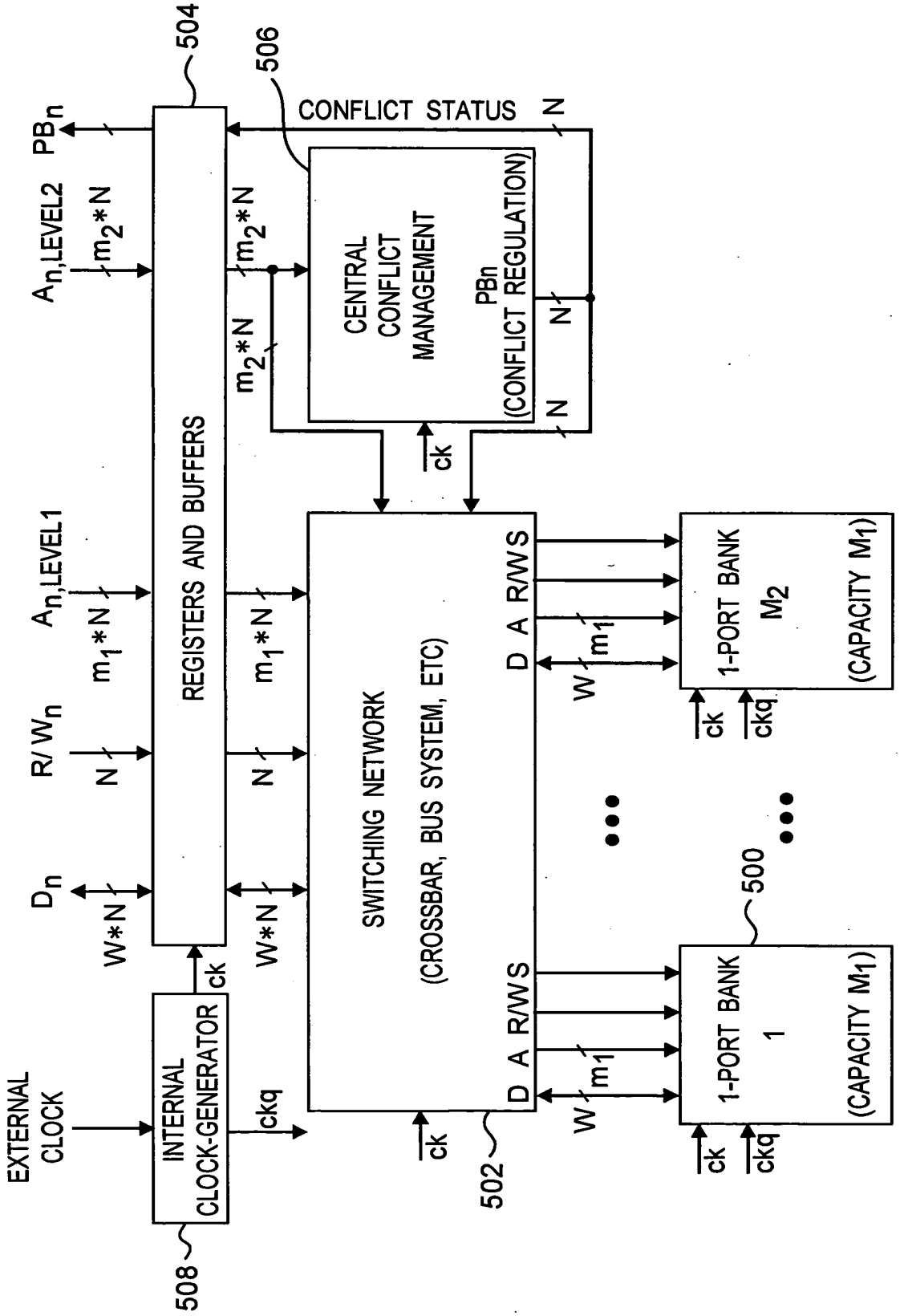

EXTERNAL CLOCK
INTERNAL CLOCK-GENERATOR
ck
ckq
508
REGISTERS AND BUFFERS
504
506
CONFLICT STATUS
N
CENTRAL CONFLICT MANAGEMENT
PBn (CONFLICT REGULATION)
N
N
ck
PBn
An,LEVEL2
m2*N
m2*N
m2*N
An,LEVEL1
m1*N
m1*N
R/Wn
N
N
Dn
W*N
W*N
SWITCHING NETWORK
(CROSSBAR, BUS SYSTEM, ETC)
ck
502
D A R/WS
D A R/WS
W
m1
W
m1
1-PORT BANK
M2
(CAPACITY M1)
1-PORT BANK
1
(CAPACITY M1)
500
ck
ckq
ck
ckq

Fig.19

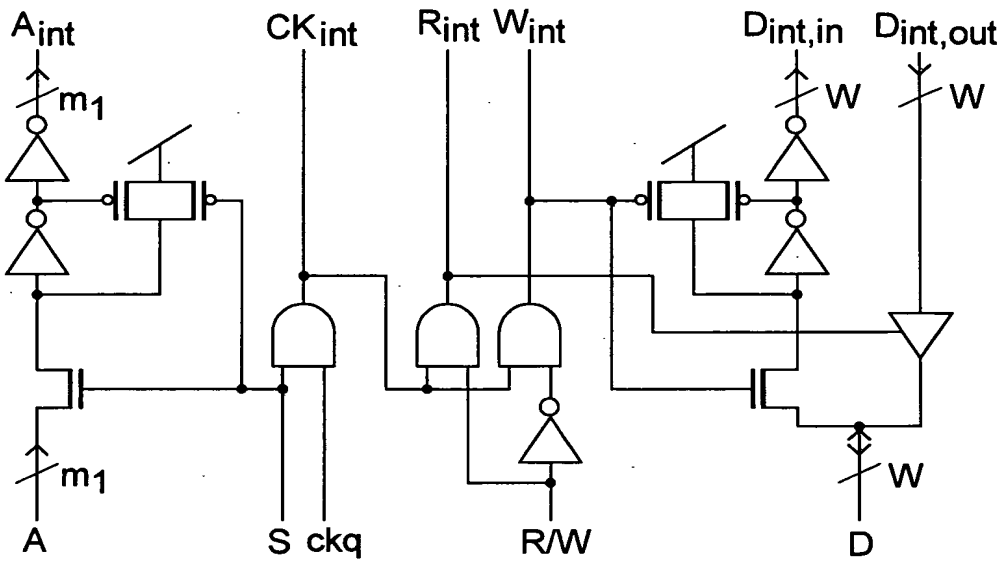


Fig.20

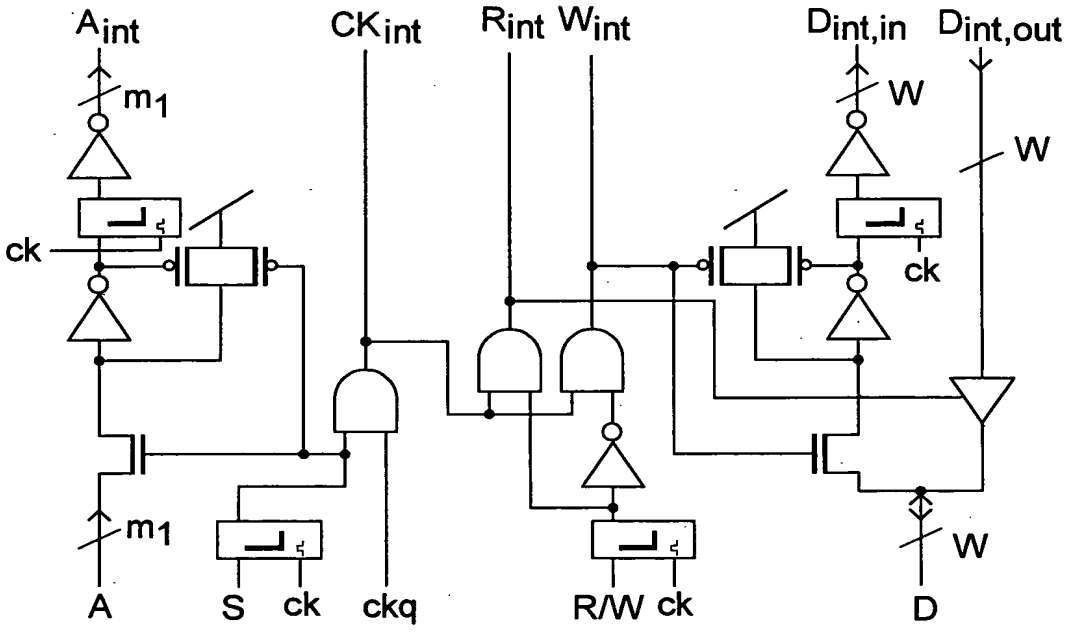

A_int
CK_int
R_int W_int
D_int,in
D_int,out
m1
W
W
ck
ck
m1
W
A
S
ck
ckq
R/W ck
D

Fig.21

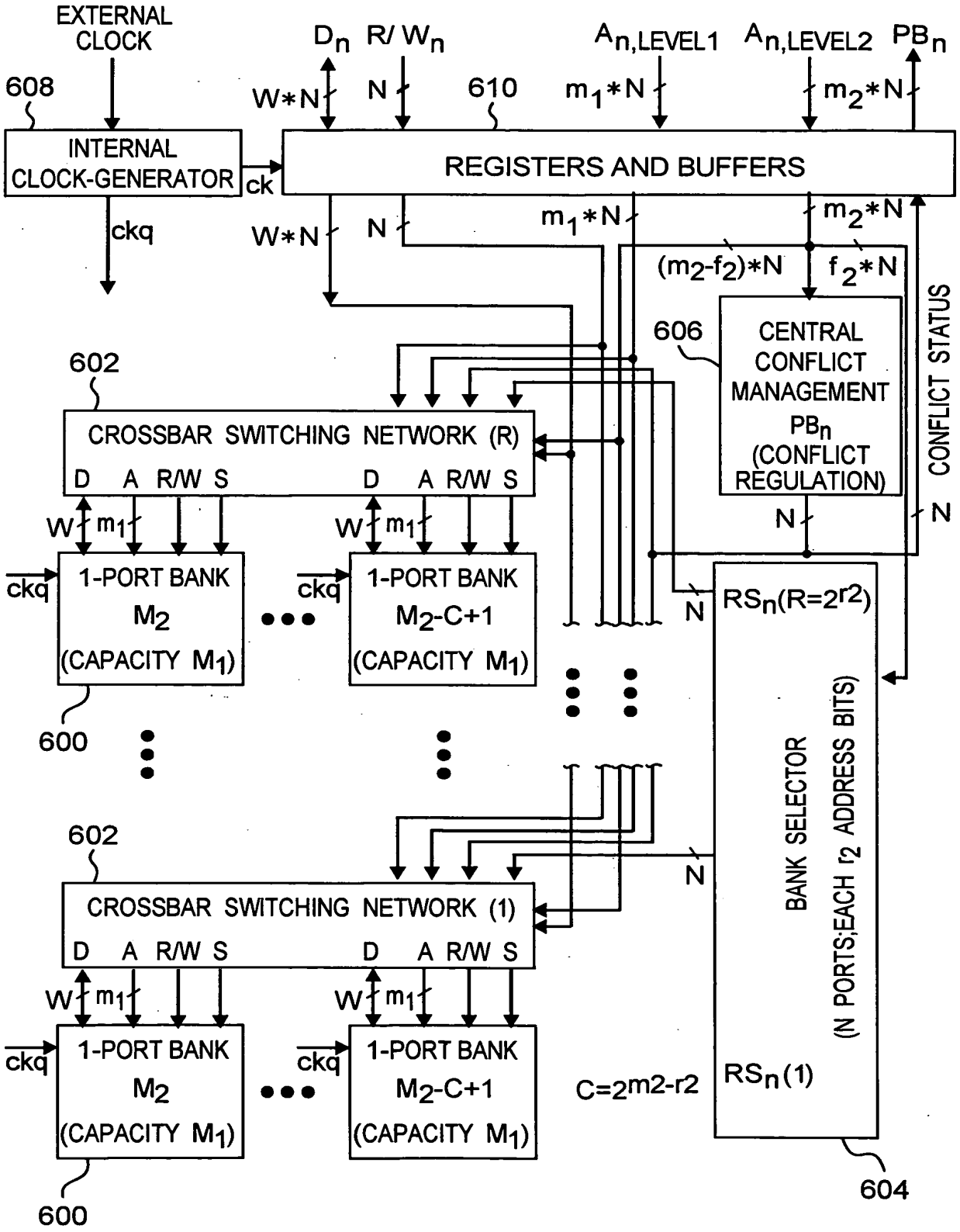

EXTERNAL CLOCK
608
INTERNAL CLOCK-GENERATOR
ck
ckq
D_n R/ W_n
W*N
N
610
REGISTERS AND BUFFERS
$A_{n,LEVEL1}$
m_1*N
$A_{n,LEVEL2}$
m_2*N
PB_n
CONFLICT STATUS
N
m_1*N
m_2*N
(m_2-f_2)*N
f_2*N
606
CENTRAL CONFLICT MANAGEMENT
PB_n
(CONFLICT REGULATION)
602
CROSSBAR SWITCHING NETWORK (R)
D A R/W S
D A R/W S
W
m_1
1-PORT BANK
M_2
(CAPACITY M_1)
1-PORT BANK
M_2-C+1
(CAPACITY M_1)
600
$RS_n(R=2^{r2})$
BANK SELECTOR
(N PORTS;EACH r_2 ADDRESS BITS)
$RS_n(1)$
$C=2^{m2-r2}$
604
CROSSBAR SWITCHING NETWORK (1)

Fig.22

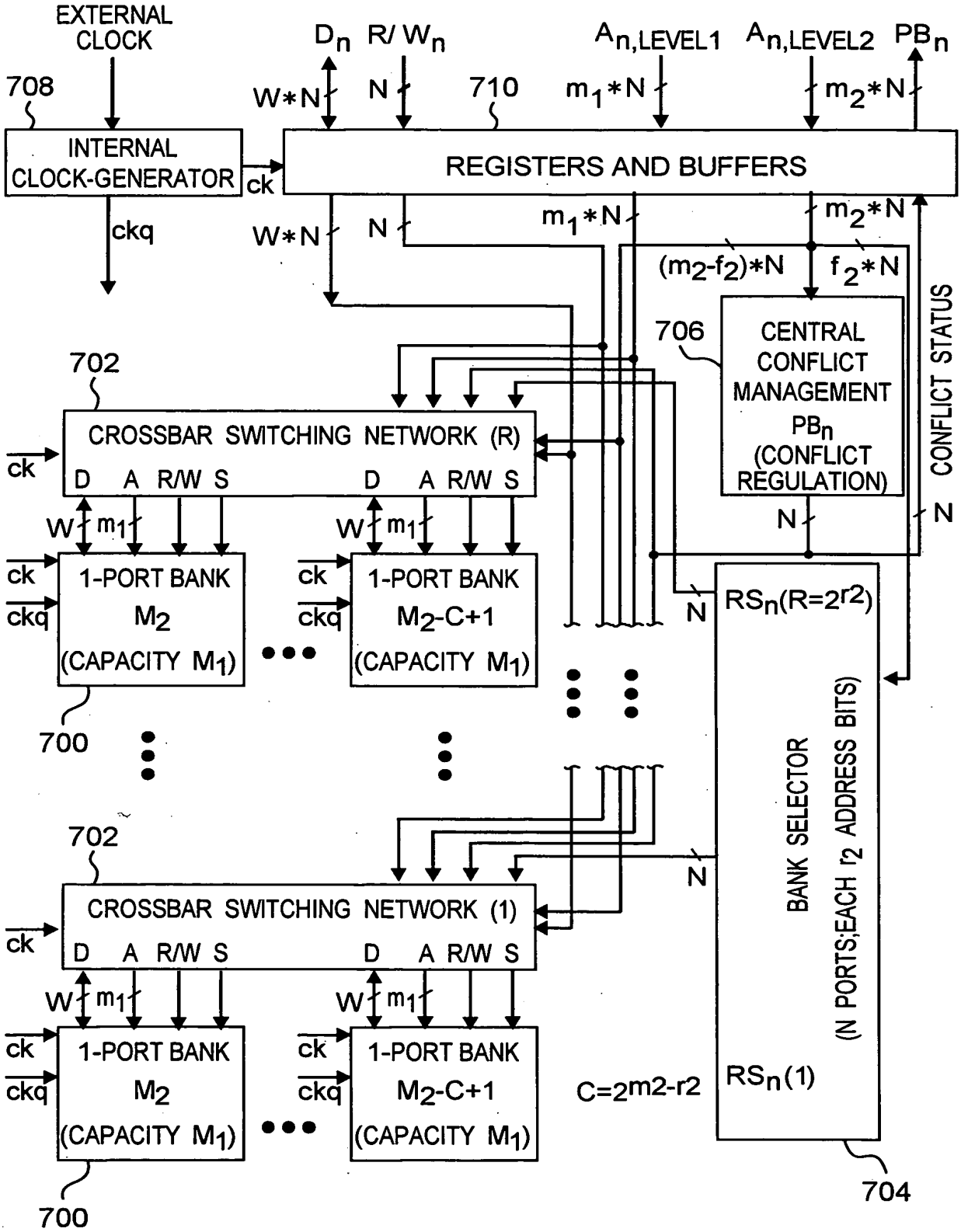
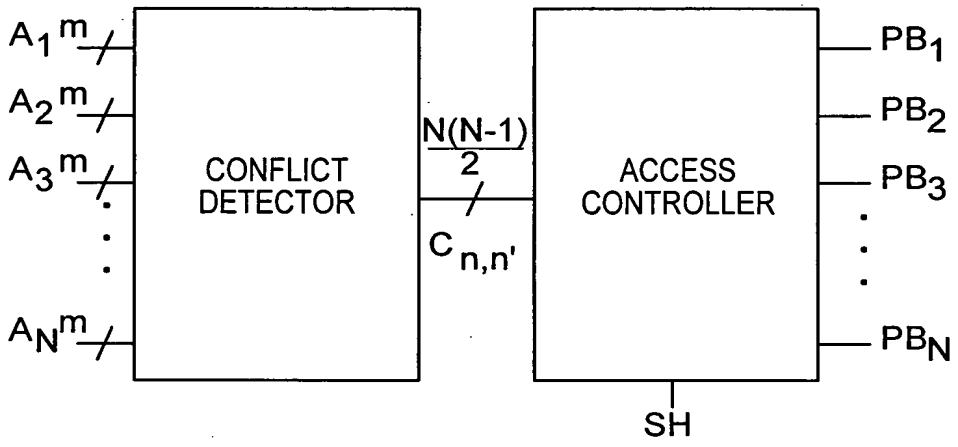

EXTERNAL CLOCK
708
INTERNAL CLOCK-GENERATOR
ck
ckq
D_n R/ W_n
W*N
N
710
REGISTERS AND BUFFERS
$A_{n,LEVEL1}$
$A_{n,LEVEL2}$
PB_n
m_1*N
m_2*N
(m_2-f_2)*N
f_2*N
CONFLICT STATUS
706
CENTRAL CONFLICT MANAGEMENT
PB_n (CONFLICT REGULATION)
702
CROSSBAR SWITCHING NETWORK (R)
D A R/W S
W
m_1
1-PORT BANK M_2 (CAPACITY M_1)
1-PORT BANK M_2-C+1 (CAPACITY M_1)
700
$RS_n(R=2^{r2})$
BANK SELECTOR
(N PORTS;EACH r_2 ADDRESS BITS)
CROSSBAR SWITCHING NETWORK (1)
$RS_n(1)$
$C=2^{m2-r2}$
704

Fig.23



A_i : BLOCK ADDRESS

m : BLOCK ADDRESS BIT NUMBER

SH : EXTERNAL CONTROL SIGNAL

$C_{n,n'}$: CONFLICT DETECTION SIGNAL

PB_n : PORT BLOCK SIGNAL

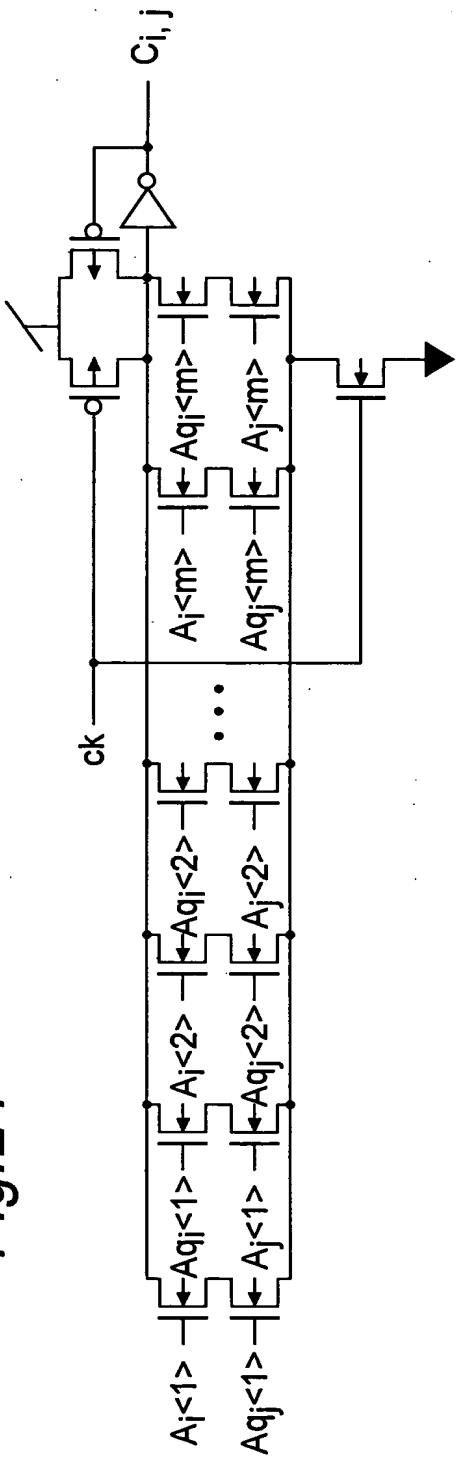


Fig.24

Fig.25

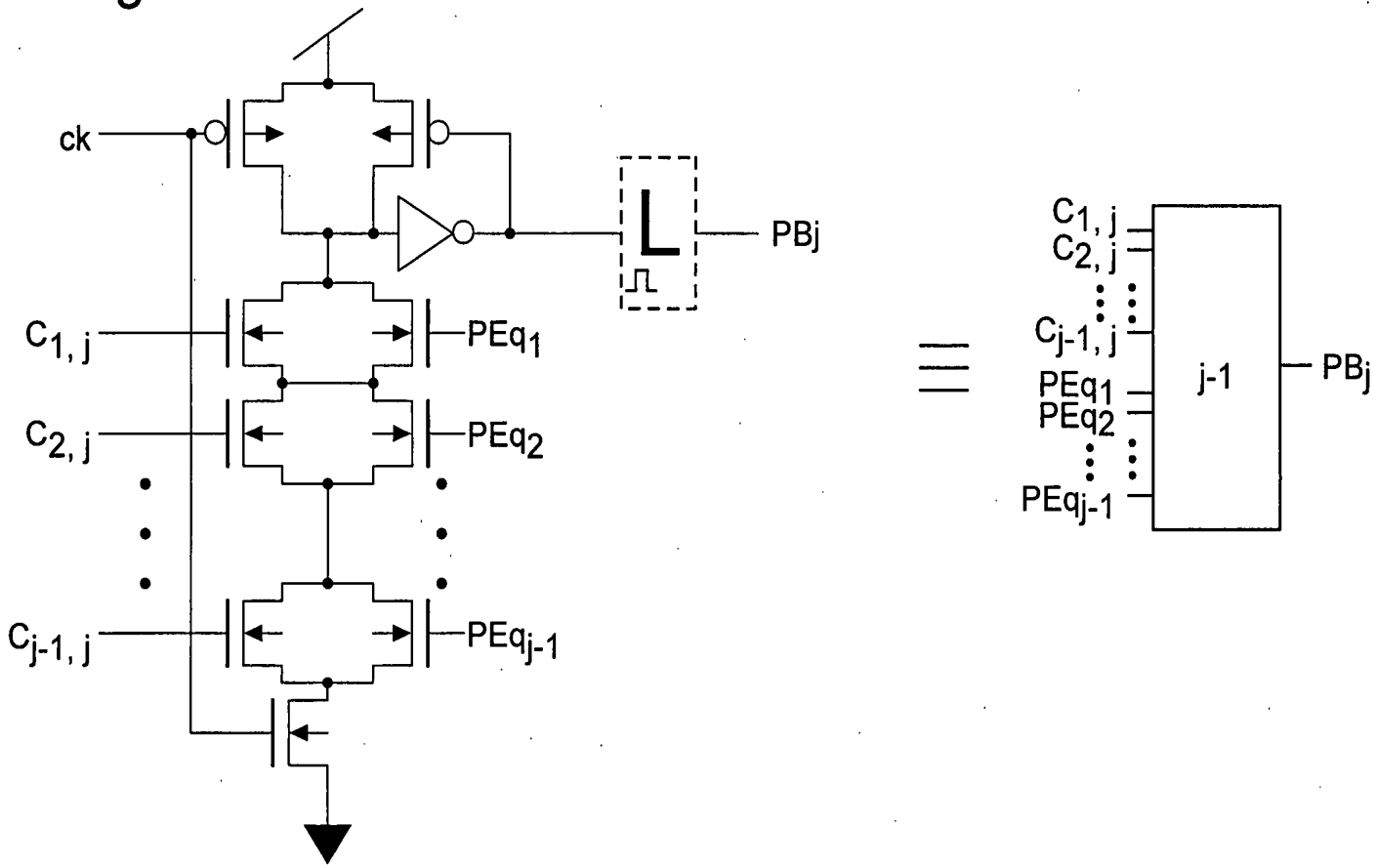

ck
PBj
C1, j
PEq1
C2, j
PEq2
Cj-1, j
PEqj-1
C1, j
C2, j
Cj-1, j
PEq1
PEq2
PEqj-1
j-1
PBj

Fig.26

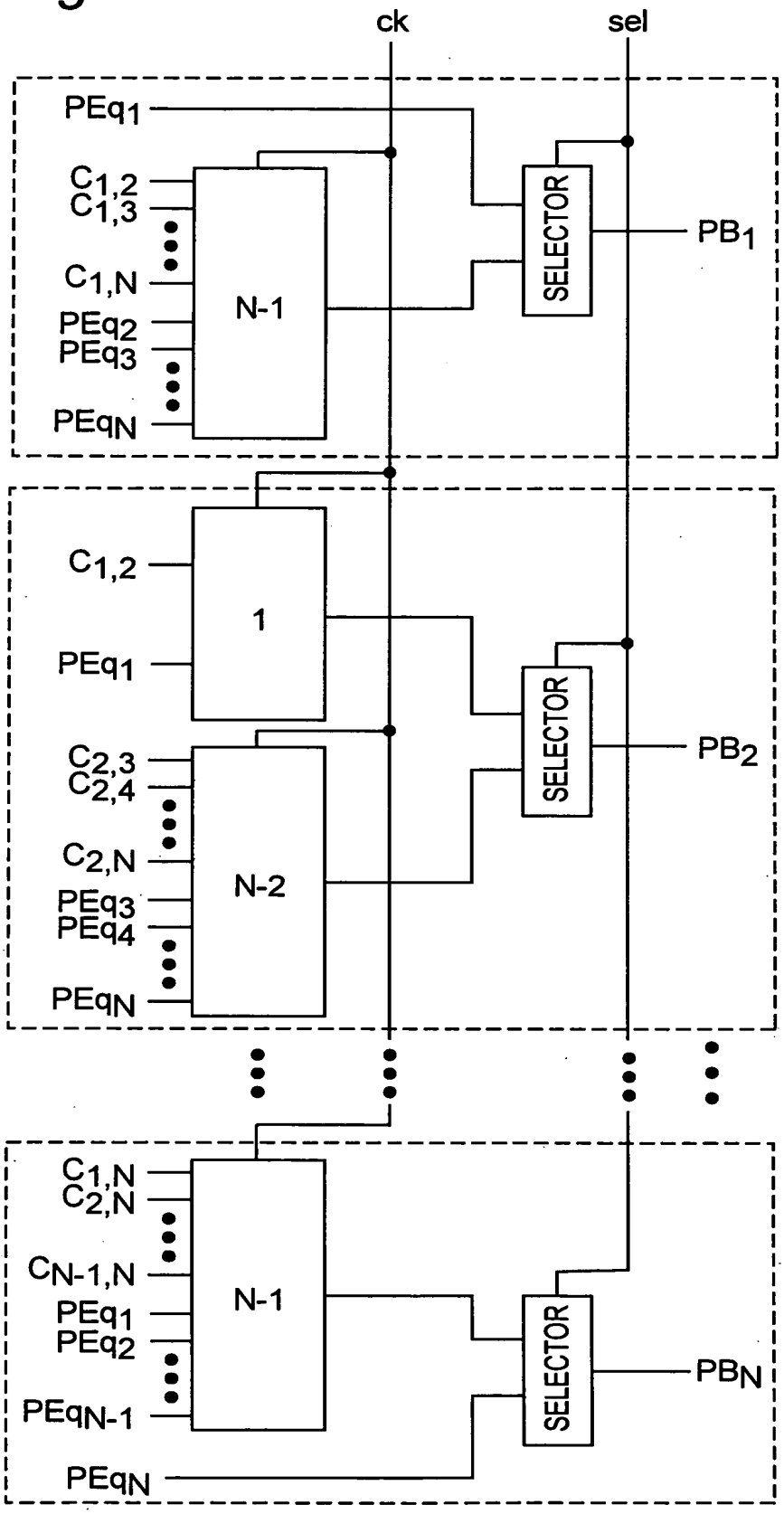

ck
sel
PEq1
C1,2
C1,3
C1,N
PEq2
PEq3
PEqN
N-1
SELECTOR
PB1
C1,2
1
PEq1
C2,3
C2,4
C2,N
PEq3
PEq4
PEqN
N-2
SELECTOR
PB2
C1,N
C2,N
CN-1,N
PEq1
PEq2
PEqN-1
PEqN
N-1
SELECTOR
PBN

Fig.27

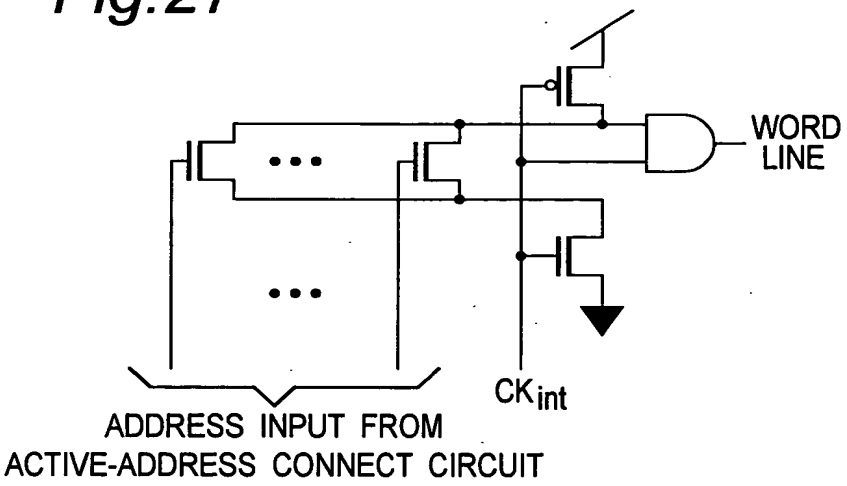

WORD LINE
CK$_{int}$
ADDRESS INPUT FROM
ACTIVE-ADDRESS CONNECT CIRCUIT

Fig.28

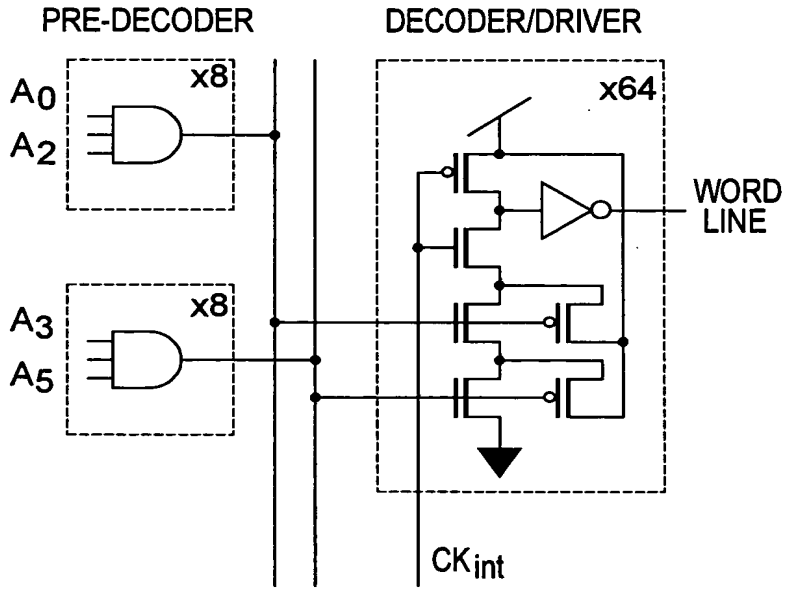

PRE-DECODER
DECODER/DRIVER
A$_0$
A$_2$
x8
A$_3$
A$_5$
x8
x64
WORD LINE
CK$_{int}$

Fig.29